GOVERNMENT OF TAMILNADU

DIRECTORATE OF TECHNICAL EDUCATION, CHENNAI-25

STATE PROJECT COORDINATION UNIT

(Established under Canada India Institutional Cooperation Project)

CURRICULUM

Course Name	**VLSI DESIGN**
Course Code	**EC/2020/022**
Course Duration	60 Hours
Minimum Eligibility Criteria	10th/+2 /ITI/Diploma/Graduate
Pre-requisites (if any)	Knowledge of Digital Electronics
Course Objectives	Training module has been designed for the participants to • Study the concept of VLSUI design. • Understand the different design steps required to carry out a complete digital VLSI (Very-Large-Scale Integration) design in silicon.
Course Outcomes	At the end of training, the trainees will be able to • Create models of moderately sized CMOS circuits that realize specified digital functions • apply CMOS technology-specific layout rules in the placement and routing of transistors and interconnect, and to verify the functionality, timing, power, and parasitic effects.
Expected Job Roles	VLSI Circuit Designer

TEACHING AND SCHEME OF EXAMINATION

Course Code	Course Name	Hours		Assessment Marks		Duration of Examination
				Min	Max	
EC/2020/022	VLSI DESIGN	Theory	24	10	20	3 Hours
		Practical	36	40	80	
		Total	60	50	100	

EC/2020/022 – VLSI DESIGN

DETAILED SYLLABUS

Unit No	Modules	No.of.Hours	
		Theory	Practical
I	**IntroductionTO VLSI**	08 Hours	
1.1	VLSI Design Flow and Y-Chart, Front-Back End VLSI Design Example, Fully Custom and Semi Custom	06	02
1.2	VLSI Design Process, VLSI-EDA Hardware-Software tools available, comparisons and their applications		
1.3	VLSI-EDA Hardware-Software tools used in Industries		
1.4	Why Verilog, Its Types-Verilog, Verilog-A and System Verilog and Simple Logic Gates Coding, Compilation and Execution in System Verilog		
II	**Programmable Logic Devices (PLDS)**	08 Hours	
2.1	Introduction, PLDs Types-Simple PLDs (SPLDs), Complex PLDs (CPLDs) and Field Programmable Gate Array (FPGA)	06	02
2.2	Architecture Details and Comparison w.r.t. Logic Blocks (CLBs), Logic Cells, System Gates, I/O Pins, Flip-Flops, Max Internal Frequency, Supply Voltage, Interconnects, Technology Used, SRAM Bits (Block RAM)		
III	**System Verilog code structure and FPGA implementation**	24 Hours	
3.1	Module Declaration, Lexical Conventions, Data Types, Analog Block Statements **Practical:** Example Program	06	18
3.2	**Practical:**Mathematical Functions and Operators, Analog Operators, Filters and Events, System Verilog Pre-processor – Example Program		
3.3	**Practical:**Verilog-FPGA Interfacing and Simulation Techniques, System Task and Input Output Functions with Example		
3.4	**Practical:**Simple Analog and Mixed System Design Practices		

IV	Spice Modelling For VLSI Design	20 Hours	
4.1	SPICE Tutorials and Commands, Sources and Passive Components	06	14
4.2	CMOS Inverter Transient Analysis, Level-1, Level-2 and Level-3 Models, BSIM Models, Diffusion Capacitance Models		
4.3	SPICE Modelling for I-V Characteristics, Threshold Voltage, Gate Capacitance, Parasitic Capacitance, Effective Resistance, path Simulation		
4.4	DC Transfer Characteristics, Logical efforts, Power and Energy Calculation, Monte Carlo Simulation, **Practical**: Simple Design Examples.		
	Total theory / Practical Hours	**24**	**36**
	Total hours	**60**	

HARDWARE REQUIREMENT

S.NO	LIST OF TOOLS /EQUIPMENTS
1	Microprocessor
2	Memory chips
3	VLSI devices

SOFTWARE REQUIREMENT

S.NO	LIST OF TOOLS
1	IC layout designing
2	Mentor graphics tool
3	Tanner

REFERENCE BOOKS

S.NO	NAME OF THE BOOK	AUTHOR	PUBLISHER
1	CMOS VLSI Design: A Circuits and Systems Perspective	Weste, Neil H. E. Weste	Pearson Education India
2	Low-Power VLSI Circuits and Systems	Ajit Pal	Springer
3	Computer Aids for VLSI Design	Steven M. Rubin	R. L. Ranch Press, 2009

ASSESSMENT AND CERTIFICATION

S.No	Criteria for assessment
1.	A trainee will be assessed based on the performance in End Examination for Theory and Practical conducted internally in the CIICP Project Polytechnic College for a duration of 3 hours
2.	A trainee must have 75% of attendance to appear for End examination in Theory and Practical.
3.	The assessment for theory part will be based on the marks scored in the end examination on the knowledge bank of questions (1 word/objective type questions)
4.	The assessment for practical part will be based on the marks scored in the end examination conducted by the CIICP Project Polytechnic and assessed by the Examiners approved by Strategic Plan Implementation Committee (SPIC) of the project polytechnic.
5.	The passing criteria for successful completion of training is every trainee should score 50% of marks in theory and practical examination.
6.	On successful completion of training, certificate will be issued to the participants by the Directorate of Technical Education through the Project Polytechnics.

END EXAMINATION

ALLOCATION OF MARKS

S.NO	Description	Max. Marks
1.	Theory Examination	20
2.	Practical Examination	
	a)Objective and Circuit Diagram	20
	b)Procedure and Connections / Execution	20
	c)Result and Viva	20
	d)Record	20
	Total Marks	**100**

THEORY MODEL QUESTION PAPER

EC/2020/022 – VLSI DESIGN

(Maximum Marks: 20)

(N.B: Answer any Twenty questions) **20x1= 20 Marks**

1. What is combinational circuit?
2. What are the universal gates?
3. Expand SOP and POS.
4. Expand VLSI and VHDL.
5. Define
6. What is CAD?
7. Write VHDL code for NOT gate.
8. List some logical operators.
9. Develop VHDL code for NAND gate.
10. Define sequential circuit.
11. Draw the excitation table for JKFF.
12. Give example for sequential circuit.
13. List difference between combinational and sequential circuit.
14. Explain design steps
15. Write VHDL code for D flip flop.
16. Define counter.
17. Mention the types of PLD.
18. State the advantages of PLD.
19. What is an ASIC.
20. Give example for ASIC.
21. Expand FPGA and CPLD.
22. Compare FPGA and CPLD.
23. Give one application of FPGA and CPLD.
24. Give example for storage element.
25. Who is father of VLSI